IN THE CLAIMS:

1. (Original) An apparatus comprising:

a memory configured to store an indication of one or more addresses, wherein the memory is coupled to receive a first address of a read command; and

a control circuit coupled to the memory, wherein the control circuit is configured to cause an issuance of one or more probes corresponding to the read command responsive to the first address missing in the memory, and wherein the control circuit is configured to inhibit the issuance of one or more probes corresponding to the read command responsive to the first address hitting in the memory.

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2. (Original) The apparatus as recited in claim 1 wherein, if the first address misses in the memory and the one or more probes result in clean probe responses, the control circuit is configured to store an indication of the first address in the memory.

3. (Original) The apparatus as recited in claim 2 wherein, in response to a second command for exclusive access to a block corresponding to the first address, the control circuit is configured to invalidate the indication of the first address in the memory.

4. (Original) The apparatus as recited in claim 3 wherein the control circuit is further configured to cause the issuance of one or more probes for the second command.

5. (Original) The apparatus as recited in claim 2 wherein the control circuit is coupled to receive an indication of a message from a source of the read command indicating whether or not the one or more probes resulted in clean probe responses.

6. (Original) The apparatus as recited in claim 1 wherein the control circuit is configured to cause a source of the read command to store a block addressed by the first address in a shared state if the first address hits in the memory.

7. (Original) The apparatus as recited in claim 6 wherein the control circuit is configured to cause an indication in a read response message transmitted to the source to indicate shared.

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8. (Original) The apparatus as recited in claim 6 wherein the control circuit is configured to cause an indication in a read response message transmitted to the source to indicate that no probe responses will be received by the source.

9. (Original) A computer system comprising:

a first node configured to transmit a read command having a first address; and

a second node coupled to receive the read command, the second node coupled to a first memory storing a first block addressed by the first address, wherein the second node includes a second memory configured to store an indication of one or more addresses, and wherein the second node is configured to issue one or more probes corresponding to the read command responsive to the first address missing in the memory, and wherein the second node is configured to inhibit the issuance of one or more probes corresponding to the read command responsive to the first address hitting in the memory.

10. (Original) The computer system as recited in claim 9 wherein, if the first address misses in the second memory and the one or more probes result in clean probe responses, the second node is configured to store an indication of the first address in the first memory.

11. (Original) The computer system as recited in claim 10 wherein, in response to a second command for exclusive access to the first block, the second node is configured to invalidate the indication of the first address in the second memory.

12. (Original) The computer system as recited in claim 11 wherein the second node is further configured to issue one or more probes for the second command.

13. (Original) The computer system as recited in claim 10 further comprising one or more nodes coupled to receive the one or more probes, wherein the one or more nodes are configured to transmit the probe responses to the first node, and wherein the first node is configured to transmit a message to the second node indicating whether or not the one or more probes resulted in clean probe responses.

14. (Original) The computer system as recited in claim 9 wherein the second node is configured to transmit the first block to the first node as a read response message, and wherein the second node is configured to indicate, in the read response message, that the first node is to store the first block in a shared state responsive to the first address hitting in the second memory.

15. (Original) The computer system as recited in claim 14 wherein the second node is further configured to indicate, in the read response message, that no probe responses will be received by the source responsive to the first address hitting in the second memory.

16. (Previously Presented) A method comprising:

receiving a first address of a read command;

searching a memory configured to store an indication of one or more addresses

for the first address;

if the searching results in a miss, transmitting one or more probes corresponding to the read command; and

if the searching results in a hit, not transmitting the one or more probes.

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17. (Original) The method as recited in claim 16 further comprising, if the searching results in a miss and the one or more probes result in clean probe responses, storing an indication of the first address in the memory.

18. (Original) The method as recited in claim 16 further comprising:

receiving a second command for exclusive access to a block corresponding to the first address; and

invalidating the indication of the first address in the memory responsive to the receiving.

19. (Original) The method as recited in claim 16 further comprising:

transmitting a read response message with a block corresponding to the first address; and

indicating, in the read response message, that a source of the read command is to store the block in a shared state.

20. (Original) The method as recited in claim 19 further comprising indicating, in the read response message, that no probe responses will be received corresponding to the read command.

21. (Previously Presented) A computer system comprising:

a first processing node configured to transmit a read command having a first address; and

a second processing node, including a directory memory and a coherency control circuit, configured to receive the read command, wherein said directory memory is coupled to said coherency control circuit, wherein said directory memory is configured to store an indication of one or more addresses and configured to receive the first address of the read command, wherein the coherency control circuit is configured to selectively issue one or more probe commands corresponding to the read command depending on whether the directory memory includes an indication of the first address.

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22. (Previously Presented) The computer system of claim 21, wherein the directory memory is a cache.

23. (Previously Presented) The computer system of claim 21, wherein the coherency control circuit is configured to cause a transmission of the one or more probe commands if the first address of the read command is a miss, wherein a miss indicates that the directory memory does not include the indication of the first address.

24. (Previously Presented) The computer system of claim 21, wherein the coherency control circuit, responsive to the first address of the read command being a hit, does not transmit of the one or more probe commands, wherein a hit indicates that the directory memory includes the indication of the first address.

25. (Currently Amended) The apparatus as recited in claim ~~1~~ 21 wherein, if the first address misses in the memory and the one or more probes result in clean probe

responses, the coherency control circuit is configured to store an indication of the first address in the memory.

~~27.~~ 26. (Currently Amended) The apparatus as recited in claim ~~2~~ 25 wherein, in response to a second command for exclusive access to a block corresponding to the first address, the coherency control circuit is configured to invalidate the indication of the first address in the memory.

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~~28.~~ 27. (Currently Amended) The apparatus as recited in claim ~~3~~ 26 wherein the coherency control circuit is further configured to cause the issuance of one or more probes for the second command.

~~29.~~ 28. (Currently Amended) The apparatus as recited in claim ~~2~~ 25 wherein the coherency control circuit is coupled to receive an indication of a message from a source of the read command indicating whether or not the one or more probes resulted in clean probe responses.

~~30.~~ 29. (Currently Amended) The apparatus as recited in claim ~~1~~ 21 wherein the coherency control circuit is configured to cause a source of the read command to store a block addressed by the first address in a shared state if the first address hits in the memory.

~~31.~~ 30. (Currently Amended) The apparatus as recited in claim ~~6~~ 29 wherein the coherency control circuit is configured to cause an indication in a read response message transmitted to the source to indicate shared.

~~32.~~ 31. (Currently Amended) The apparatus as recited in claim ~~6~~ 29 wherein the coherency control circuit is configured to cause an indication in a read response message transmitted to the source to indicate that no probe responses will be received by the source.